Refine Search

Search Results -

Terms	Documents
L1 same (port near5 program$5)	18

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
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Derwent World Patents Index
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Search: L3

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Recall Text | Clear | Interrupt

Search History

DATE: Thursday, June 02, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	L1 same (port near5 program$5)	18	L3
L2	L1 same port	120	L2
L1	(program$5 near5 (device or module or unit)) same (processor or microprocessor) same bus same configur$5 same ((I adj1 O) or (input adj1 output) or peripheral)	602	L1

END OF SEARCH HISTORY

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Search Results -

Terms	Documents
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IBM Technical Disclosure Bulletins

Search: L4

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Search History

DATE: Thursday, June 02, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	L1 same (port near5 program$5)	18	L3
L2	L1 same port	120	L2
L1	(program$5 near5 (device or module or unit)) same (processor or microprocessor) same bus same configur$5 same ((I adj1 O) or (input adj1 output) or peripheral)	602	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L3	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
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Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Thursday, June 02, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	L1 same (port near5 program$5)	18	L3
L2	L1 same port	120	L2
L1	(program$5 near5 (device or module or unit)) same (processor or microprocessor) same bus same configur$5 same ((I adj1 O) or (input adj1 output) or peripheral)	602	L1

END OF SEARCH HISTORY

Results for "(programmable logic device<in>metadata) and microprocessor and port and bus"

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(programmable logic device<in>metadata) and microprocessor and port and bus >>

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Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Select Article Information

1. **An Undergraduate System-on-Chip (SoC) Course for Computer Engineering Students**
Bindal, A.; Mann, S.; Ahmed, B.N.; Raimundo, L.A.;
Education, IEEE Transactions on
Volume 48, Issue 2, May 2005 Page(s):279 - 289
AbstractPlus | Full Text: PDF(1016 KB) IEEE JNL

2. **Bus I/O register intensive user-configurable microprocessor peripheral**
Hung, C.-Y.; Chan, Y.-F.;
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16-19 May 1988 Page(s):15.5/1 - 15.5/4
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3. **A VHDL-based methodology to develop high performance servo drivers**
Pimentel, J.C.G.; Le-Huy, H.;
Industry Applications Conference, 2000. Conference Record of the 2000 IEEE
Volume 3, 8-12 Oct. 2000 Page(s):1505 - 1512 vol.3
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4. **Simulation tools for digital design and computer organization and architecture**
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6. **Implementation of microprogrammed control in FPGAs**
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Industrial Electronics, IEEE Transactions on
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7. **Rapid prototyping using field-programmable logic devices**
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Volume 20, Issue 3, May-June 2000 Page(s):29 - 37

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8. **In-circuit-emulation in ASIC architectural core designs**
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9. **Design of a microcomputer platform with real-time operating system for laboratory projects**
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Volume 3, 5-8 Nov. 1997 Page(s):1383 - 1387 vol.3

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10. **A CPLD design of a self-organizing system for data clustering**
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Volume 2, 31 May-3 June 1998 Page(s):441 - 444 vol.2

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11. **The design and implementation of microcontroller supported amalgamator [for dentistry]**
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Electrotechnical Conference, 2000. MELECON 2000. 10th Mediterranean
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12. **Development and testing of an acoustic positioning system - description and signal processing**
de Lima, F.V.F.; Furukawa, C.M.;
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13. **Control of excitation block applied in an electronic beam scanning radar system, concept and implementation**
Kucy, K.;
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Volume 2, 20-22 May 2002 Page(s):643 - 646 vol.2

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12-15 May 2002

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15. **Power efficiency through application-specific instruction memory transformations**
Petrov, P.; Orailoglu, A.;
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16. **Design issues for prototype implementation of a pipelined superscalar processor in programmable logic**
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22-26 April 2003 Page(s):11 pp.

AbstractPlus | Full Text: PDF(368 KB) IEEE CNF

Bus I/O register intensive user-configurable microprocessor peripheral

Hung, C.-Y. Chan, Y.-F.
Altera Corp., Santa Clara, CA, USA ;

This paper appears in: **Custom Integrated Circuits Conference, 1988., Proceedings of the IEEE 1988**
Publication Date: 16-19 May 1988
On page(s): 15.5/1 - 15.5/4
Meeting Date: 05/16/1988 - 05/19/1988
Location: Rochester, NY
INSPEC Accession Number:3257530
DOI: 10.1109/CICC.1988.20874
Posted online: 2002-08-06 15:59:41.0

Abstract
A CMOS erasable **programmable logic device** (EPLD) optimized for **microprocessor** peripheral and **bus** control applications is described. In addition to a general-purpose EPLD core and 52 user-configurable registers, the dedicated peripheral I/O logic can be programmed by the control macrocells to interface directly to all known **microprocessor** families. An I/O **bus port** with 24-mA drive capability allows direct connection to a **microprocessor bus**

Index Terms
Inspec

Controlled Indexing
CMOS integrated circuits cellular arrays integrated logic circuits

Non-controlled Indexing
24 mA 24-mA drive capability CMOS EPLD I/O bus port I/O register intensive bus control applications bus interface direct interfacing erasable **programmable logic device** general-purpose EPLD core macrocells peripheral interface user-configurable **microprocessor** peripheral user-configurable registers

Author Keywords
Not Available

References

No references available on IEEE Xplore.

Citing Documents

No citing documents available on IEEE Xplore.

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L3: Entry 1 of 18 File: PGPB Feb 12, 2004

DOCUMENT-IDENTIFIER: US 20040030861 A1
TITLE: Customizable computer system

Summary of Invention Paragraph:
[0005] In a first embodiment of the invention there is provided a customizable computing system, having a microprocessor and a programmable logic device coupled to the microprocessor via a dedicated bus. The microprocessor and the programmable logic device may be integrated within the same physical package, but are separate components. In some embodiments, the dedicated bus includes a request path that is 32 bits wide. The programmable logic device includes a configuration to provide I/O functionality to the system and may be a field programmable gate array. The programmable logic device operates as both a north bridge and a south bridge as is understood by those of ordinary skill in the art. The system further includes a system port coupled to the programmable logic device. In another embodiment, the system further includes a second bus coupled to the programmable logic device, wherein the system port is coupled to the second bus. The system may also have a plurality of ports coupled to the gate array and the ports may be coupled to the second bus.

CLAIMS:

1. A customizable computing system, the system comprising: a microprocessor; a programmable logic device coupled to the microprocessor via a dedicated bus, and wherein the programmable logic device includes a configuration to provide I/O functionality to the system and includes one or more I/O interfaces; and a system port coupled to the programmable logic device.

L3: Entry 1 of 18 File: PGPB Feb 12, 2004

PGPUB-DOCUMENT-NUMBER: 20040030861
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040030861 A1

TITLE: Customizable computer system

PUBLICATION-DATE: February 12, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Plackle, Bart	Diest		BE	
Herremans, Kurt	Hasselt		BE	

APPL-NO: 10/ 609141 [PALM]
DATE FILED: June 27, 2003

RELATED-US-APPL-DATA:
Application is a non-provisional-of-provisional application 60/392344, filed June 27, 2002,

INT-CL: [07] G06 F 15/00, G06 F 15/76

US-CL-PUBLISHED: 712/32
US-CL-CURRENT: 712/32

REPRESENTATIVE-FIGURES: 2

ABSTRACT:

A customizable computing system, having a microprocessor and a programmable logic device coupled to the microprocessor via a dedicated bus. The programmable logic device includes a configuration to provide I/O functionality to the system and may be a field programmable gate array. The programmable logic device operates as both a north bridge and a south bridge as is understood by those of ordinary skill in the art. Requests are received from the microprocessor in the programmable logic device over the dedicated bus and are processor specific requests. The processor specific requests are translated into processor dependent commands by a bridge. After the processor specific requests are translated into processor dependent commands, the commands are forwarded to processor independent I/O structures which interface with both internal and external peripheral devices to the customizable computing system.

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This U.S. patent application claims priority from provisional patent application Serial No. 60/392,344 filed on Jun. 27, 2002 entitled "Customizable Computer System" and bearing attorney docket 2684/102 which is incorporated herein by reference in its entirety.

L3: Entry 17 of 18 File: USPT Apr 26, 1994

DOCUMENT-IDENTIFIER: US 5307463 A

** See image for Certificate of Correction **

TITLE: Programmable controller communication module

Brief Summary Text (11):

A module controller supervises the transfer of data within the module among the I/O ports and backplane bus of a rack for the programmable controller into which the communication interface module is incorporated. The module controller inspects an incoming message and determines if it is destined to be forwarded over another communication link, in which case the message is directed to the I/O port circuit for that other link. The message is relayed without ever being sent over the rack backplane bus and without requiring processing time from the central processor module of the programmable controller. In other instances, the module configuration data may also instruct the module controller to transfer the data to one or more of the I/O ports and the central processor in the programmable controller.

L3: Entry 17 of 18 File: USPT Apr 26, 1994

US-PAT-NO: 5307463
DOCUMENT-IDENTIFIER: US 5307463 A
** See image for Certificate of Correction **

TITLE: Programmable controller communication module

DATE-ISSUED: April 26, 1994

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hyatt; Craig S.	Pewaukee	WI		
Hostria; Emmanuel G. D.	Mukwonago	WI		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Allen-Bradley Company, Inc.	Milwaukee	WI			02

APPL-NO: 07/ 987104 [PALM]
DATE FILED: December 7, 1992

PARENT-CASE:
This application is a continuation of U.S. patent application Ser. No. 07/490,907, filed Mar. 8, 1990, now abandoned.

INT-CL: [05] G06F 13/12

US-CL-ISSUED: 395/275; 364/DIG.2, 364/927.92, 364/927.95, 364/927.99, 364/926.93, 364/940, 364/949, 364/949.91
US-CL-CURRENT: 710/1

FIELD-OF-SEARCH: 395/325, 395/200, 395/275, 395/325, 364/130, 364/140, 364/146, 364/188

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4442504	April 1984	Dummermuth et al.	395/725
☐	4631666	December 1986	Harris	395/325
☐	4787028	November 1988	Finfroch	395/325
☐	4858101	August 1989	Stewart et al.	395/275

ART-UNIT: 238

PRIMARY-EXAMINER: Chun; Debra A.

ATTY-AGENT-FIRM: Quarles & Brady

ABSTRACT:

A module interfaces a programmable controller to several serial communication networks for the exchange of data carrying messages. A central processor controls the transfer of data between the module and other programmable controller components. The module has a separate port circuit for each of the networks permitting communication using different protocols. Messages received through one port circuit can be routed to another port circuit or other programmable controller components as specified by routing data stored in the module. The module also can be configured to detect when a given sequence of data is contained in a received message or to parse a section of data from the message. In these cases, an indication of whether the data sequence was found or the parsed data is routed to a designated output of the module.

8 Claims, 9 Drawing figures

Previous Doc Next Doc Go to Doc#

L3: Entry 14 of 18 File: USPT Dec 5, 1995

DOCUMENT-IDENTIFIER: US 5473666 A

**** See image for Certificate of Correction ****

TITLE: Method and apparatus for digitally controlling gain in a talking path

Detailed Description Text (28):

FIG. 4 illustrates the details of the CPU module 56. As noted on the left of FIG. 4, the bus 100a, 100b is shown connected from a processor 122 and extended to the programmable logic devices comprising the multi-path multiplexers 98 and 101 of the I/O module 50. In the preferred form of the invention, the processor 122 comprises a Motorola 68302 microprocessor operating at 16.67 MHz. The processor 122 accommodates three synchronous/asynchronous programmable serial ports. One serial port 124 can transmit or receive serial data between the test system 10 and the 201 XL translator 40 via the communication module 35 (FIG. 1). Port 124 accommodates synchronous serial data. The second serial port 126 accommodates asynchronous data from either remote HV modules or remote SS metallic test access unit (MTAU) modules. The third serial port 128 is an asynchronous port for communicating with the local craft interface 94 (FIG. 3). The serial ports 124-126 are multi-functional ports operating at the TTL level and are configurable to operate in transmit or receive modes based on the logic state of the RTU-DIS processor input 130. As noted above, the processor 122 is supported by numerous types of memory as shown in FIG. 4, and identified above. A number of address and data buffers 132 buffer signals on the unidirectional outgoing address bus 134, as well as the bidirectional data bus 136. System reset, enable and read/write signal lines 138 are carried throughout the internal system bus with the address and data signals. An additional bus 140 is connected to the digital signal processor module 58 for interrupt and acknowledge functions. A failure of the CPU module 56 is communicated to the I/O module 10 by way of the signal line 142.

L3: Entry 14 of 18 File: USPT Dec 5, 1995

US-PAT-NO: 5473666
DOCUMENT-IDENTIFIER: US 5473666 A
** See image for Certificate of Correction **

TITLE: Method and apparatus for digitally controlling gain in a talking path

DATE-ISSUED: December 5, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Szczebak, Jr.; Edward J.	Plano	TX		
Balthrop, Sr.; Chris A.	Dallas	TX		
Mutzabaugh; Patricia K.	Garland	TX		
Porter; John M.	Fort Worth	TX		
Stewart; Gary D.	Dallas	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Reliance Comm/Tec Corporation	Bedford	TX			02

APPL-NO: 07/ 944204 [PALM]
DATE FILED: September 11, 1992

INT-CL: [06] H04 M 1/24

US-CL-ISSUED: 379/3; 379/402, 375/345
US-CL-CURRENT: 379/3; 375/345, 379/402

FIELD-OF-SEARCH: 375/98, 375/345, 379/345, 379/347, 379/402-404, 379/390, 379/3, 379/395

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3359378	December 1967	Skeer	379/344
☐	4192974	March 1980	Kiko	179/16F
☐	4331843	May 1982	Tan et al.	379/403
☐	4980908	December 1990	Yu	379/67
☐	5045809	September 1991	Cho	330/284
☐	5075687	December 1991	Chen et al.	341/110
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"Digital Data System Channel Interface Specification," Bell System Technical Reference--PUB 62310, Sep. 1983.

ART-UNIT: 264

PRIMARY-EXAMINER: Chin; Stephen

ASSISTANT-EXAMINER: Kim; Kevin

ATTY-AGENT-FIRM: Richards, Medlock & Andrews

ABSTRACT:

A processor controlled test set is disclosed for testing special service circuits of a telecommunication system. A microprocessor controls the overall operation of the test set, while a digital signal processor provides high speed timing signals to the various test circuits for generating the wave forms used in testing, as well as analyzes the test result signals that are converted into digital signals. A calibration of the test generator signals as well as the signal measuring path is carried out prior to the test sequence. The digital signal processor also provides gain control over a talking path to maintain stability thereof. An I/O circuit of the test set provides plural communication paths between remote equipment and the test set to initiate and carry out various tests. Processors in the I/O module are effective to convert the various protocols of the serial data, by way of software, to digital bit streams usable by the test set.

42 Claims, 35 Drawing figures

Previous Doc Next Doc Go to Doc#

L3: Entry 11 of 18 File: USPT Nov 3, 1998

DOCUMENT-IDENTIFIER: US 5832240 A
TITLE: ISDN-based high speed communication system

Detailed Description Text (5):
The protocol processor 44, application processor 46 and PC bus can all interrupt each other using programmable input/output (I/O) pins. Protocol processor interrupts are also used by I/O circuits described below as indicators for transferring data between the PC card 30 and the ISDN network 16. Programmable chip selects on the protocol processor 44 are used to select DRAMs located in the shared memory 40. The protocol processor 44 preferably has access to the first megabyte of the shared memory 40. The programmable chip selects are also used to select serial communication circuits 48 and 50, and to select flash read only memories (ROMs) 52 and 54. Programmable I/O bits in 62 are used to generate and clear interrupts to and from the PC and the applications processor 46. The protocol processor 44 also comprises eight programmable I/O port bits for performing such functions as controlling a diagnostic light emitting diode (LED), reading the status of interrupts to the PC and the applications processor 46, and enabling the PC serial port. Processor 44 allows autobauding for rate adaption or, optionally, for a Non-Maskable Interrupt (NMI). A second timer provides a clock for the refresh rate timer in the DMA/interrupt/refresh controller 64. A third timer is used by the protocol processor as a real time clock. Programmable logic devices (PLDs) for implementing functions 60, 62, 66 and 68 are provided on the PC card and configured to control bus operations, and port configuration and I/O operations, memory, control and arbitration, respectively. The PLDs provide control signals for controlling and enabling the address and data bus buffers associated with the applications processor 46, protocol processor 44, and PC bus interface.

L3: Entry 11 of 18 File: USPT Nov 3, 1998

US-PAT-NO: 5832240
DOCUMENT-IDENTIFIER: US 5832240 A

TITLE: ISDN-based high speed communication system

DATE-ISSUED: November 3, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Larsen; Allen J	Campbell	CA	95008	
Hergert; Jennifer K.	Campbell	CA	95008	
Brown; Charles D.	Herndon	VA	22021	
Cross; William C.	Los Gatos	CA	95030	
Dove; Ronald E.	Felton	CA	95018	
Heller; Paul W. T.	San Jose	CA	95124	

APPL-NO: 08/ 843114 [PALM]
DATE FILED: April 28, 1997

PARENT-CASE:
This application is a continuation of application Ser. No. 08/585,607, filed Jan. 11, 1996, now abandoned which is a continuation of application Ser. No. 08/225,877, filed Apr. 11, 1994, now abandoned which is, in turn, a divisional of Ser. No. 08/883,862, filed May 15, 1992 now abandoned.

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/285
US-CL-CURRENT: 710/105

FIELD-OF-SEARCH: 395/280, 395/285, 395/286, 370/94.1, 370/110.1, 379/211

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4433378	February 1984	Leger	395/325
☐	4441162	April 1984	Lillie	395/425
☐	4858112	August 1989	Puerzer et al.	395/325
☐	4884269	November 1989	Duncanson et al.	370/110.1
☐	4905237	February 1990	Voelzke	370/110.1
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☐	5329579	July 1994	Brunson	379/88
☐	5450412	September 1995	Takebayashi et al.	370/95.1
☐	5479498	December 1995	Brandman et al.	379/283

ART-UNIT: 271

PRIMARY-EXAMINER: Sheikh; Ayaz R.

ASSISTANT-EXAMINER: Wiley; David A.

ATTY-AGENT-FIRM: Burdett; James R.

ABSTRACT:

An ISDN interface is provided on a card, which is adapted for mounting in a terminal computer and which is operable to exchange data with a terminal computer and an ISDN. The ISDN interface card includes a protocol processor that is programmable to process data encoded in accordance with a number of different protocols and a digital signal processor that is programmable for data compression, encryption and facsimile applications, and u-law and a-law conversion, among other applications. The ISDN card dynamically allocates data calls between one or two B-channels to achieve a data transmission rate of 128 kbps. A power supply with a ring generator is provided to allow for the use of an analog telephone with the ISDN card. The ISDN card is programmable to allow users to create customized screens for various call processes, and to allow for the updating of a flash ROM coupled to the protocol processor through the terminal computer and the ISDN.

22 Claims, 21 Drawing figures

Previous Doc Next Doc Go to Doc#

L3: Entry 10 of 18 File: USPT Nov 6, 2001

DOCUMENT-IDENTIFIER: US 6314551 B1
TITLE: System processing unit extended with programmable logic for plurality of functions

Brief Summary Text (10):
A system is also disclosed for configuring the integrated circuit for one of a plurality of possible functions. The system comprises a computer system, the integrated circuit, and a cable for operatively coupling the computer system and the integrated circuit. The computer system preferably includes a system bus for transferring commands and data, a processor coupled to said system bus, a memory which is operable to store commands and data in a form accessible by the processor, and an I/O port coupled to said system bus. The processor is operable to execute the commands and operate on the data, and the I/O port is operable to conduct programming instructions and data in response to processor operation. The integrated circuit is coupled to the I/O port and receives the programming instructions and data from the I/O port which operates to configure the integrated circuit. The integrated circuit is configurable for a plurality of possible functions and includes a main system processing unit, a plurality of functional logic blocks, programmable logic, and a plurality of I/O pads.

L3: Entry 10 of 18 File: USPT Nov 6, 2001

US-PAT-NO: 6314551
DOCUMENT-IDENTIFIER: US 6314551 B1

TITLE: System processing unit extended with programmable logic for plurality of functions

DATE-ISSUED: November 6, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Borland; David J.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Morgan Stanley & Co. Incorporated	New York	NY			02

APPL-NO: 09/ 102465 [PALM]
DATE FILED: June 22, 1998

INT-CL: [07] H03 K 17/693, H03 K 19/173, H03 K 19/177, G06 F 7/38

US-CL-ISSUED: 716/17; 716/16, 326/37, 326/38, 326/39
US-CL-CURRENT: 716/17; 326/37, 326/38, 326/39, 716/16

FIELD-OF-SEARCH: 716/16, 716/17, 710/129, 701/36, 711/112, 712/37, 712/39, 326/37-39

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5260881	November 1993	Agrawal et al.	716/16
☐	5321845	June 1994	Sawase et al.	712/37
☐	5600845	February 1997	Gilson	712/39
☐	5640106	June 1997	Erickson et al.	326/38
☐	5644496	July 1997	Agrawal et al.	716/17
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☐	6065087	May 2000	Keaveny et al.	710/129
☐	6085285	July 2000	Lucas et al.	711/112

ART-UNIT: 278

PRIMARY-EXAMINER: Smith; Matthew

ASSISTANT-EXAMINER: Speight; Jibreel

ABSTRACT:

An integrated circuit including a main system processing unit which can be extended using a plurality of programmable logic unit for a plurality of possible functions, and a system for programming same. The integrated circuit also includes a plurality of functional logic blocks, a plurality of input/output (I/O) pads, and programmable logic coupled to each of the plurality of functional logic blocks. The main system processing unit is operable to perform a first function. Each of the plurality of functional logic blocks is operable to perform a respective function. The programmable logic is operable to route data to and from various ones of the plurality of functional logic blocks. The programmable logic is programmable to configure operation of two or more of the plurality of functional logic blocks and is also programmable to create data paths between two or of the plurality of functional logic blocks to configure the integrated circuit for one of the plurality of functions. The plurality of I/O pads is coupled to the main system processing unit and the plurality of functional logic blocks. The I/O pads are operable to transfer data signals between the integrated circuit and an external device. The programmable logic may perform a function different from each of the plurality of functional logic blocks. The system for programming the integrated circuit includes a computer system, the integrated circuit, and a cable for coupling the two.

16 Claims, 3 Drawing figures

Previous Doc Next Doc Go to Doc#

L3: Entry 8 of 18 File: USPT Jun 8, 2004

DOCUMENT-IDENTIFIER: US 6748475 B1
TITLE: Programmable serial port architecture and system

Brief Summary Text (7):
In designs requiring greater flexibility than afforded by non-programmable devices, a software programmable serial port of a conventional microprocessor may be used. For example, the Motorola M68HC11 family of microcontrollers includes a serial port known in the art as the Motorola Synchronous Serial Peripheral Interface (SPI). Such a configuration is generally shown in FIG. 1. The microcontroller 100 includes serial hardware 101 controlled by software 102, which may also communicate with a system bus 103. Serial communications occur over signal paths 104. However, such serial interfaces are disadvantageous because of several factors. Even in interfaces that are software controlled, like the SPI interface, the electrical parameters, numbers of signal paths, type of signal paths, etc. are predefined and inflexible. The processor 100 must execute a software program 102 to control the serial port, and all serial data to be sent over signal paths 104 passes through the processor 100, thus additionally loading the processor 100, above whatever load is imposed by the task for which the processor 100 is principally employed. Also, because the serial hardware 101 is a power-consuming part of the processor 100, additional power is consumed whenever the processor is executing a software program.

L3: Entry 8 of 18 File: USPT Jun 8, 2004

US-PAT-NO: 6748475
DOCUMENT-IDENTIFIER: US 6748475 B1

TITLE: Programmable serial port architecture and system

DATE-ISSUED: June 8, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
S.o slashed.rensen; J.o slashed.rn	Aars			DK

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Analog Devices, Inc.	Norwood	MA			02

APPL-NO: 09/ 706450 [PALM]
DATE FILED: November 3, 2000

PARENT-CASE:
CROSS REFERENCE TO RELATED APPLICATIONS This application claims domestic priority under 35 U.S.C. .sctn.119(e) to U.S. Provisional Patent Application Serial No. 60/163,816, filed Nov. 5, 1999, now abandoned, and incorporated herein in its entirety by reference.

INT-CL: [07] G06 F 13/00, G06 F 13/42

US-CL-ISSUED: 710/305; 710/105, 713/322, 370/463
US-CL-CURRENT: 710/305; 370/463, 710/105, 713/322

FIELD-OF-SEARCH: 710/63, 710/305, 710/100, 710/300, 710/315, 710/105, 709/250, 712/37, 370/463, 370/419, 713/600, 713/500, 713/322, 375/220

PRIOR-ART-DISCLOSED:

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☐	5442775	August 1995	Whitted, II et al.	
☐	5557751	September 1996	Banman et al.	
☐	5615404	March 1997	Knoll et al.	
☐	5628030	May 1997	Tuckner	
☐	5694555	December 1997	Morriss et al.	
☐	5809091	September 1998	Barrow	

☐	6038400	March 2000	Bell et al.
☐	6128311	October 2000	Poulis et al.
☐	6389498	May 2002	Edwards et al.

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 665 502	August 1995	EP	

ART-UNIT: 2111

PRIMARY-EXAMINER: Ray; Gopal C.

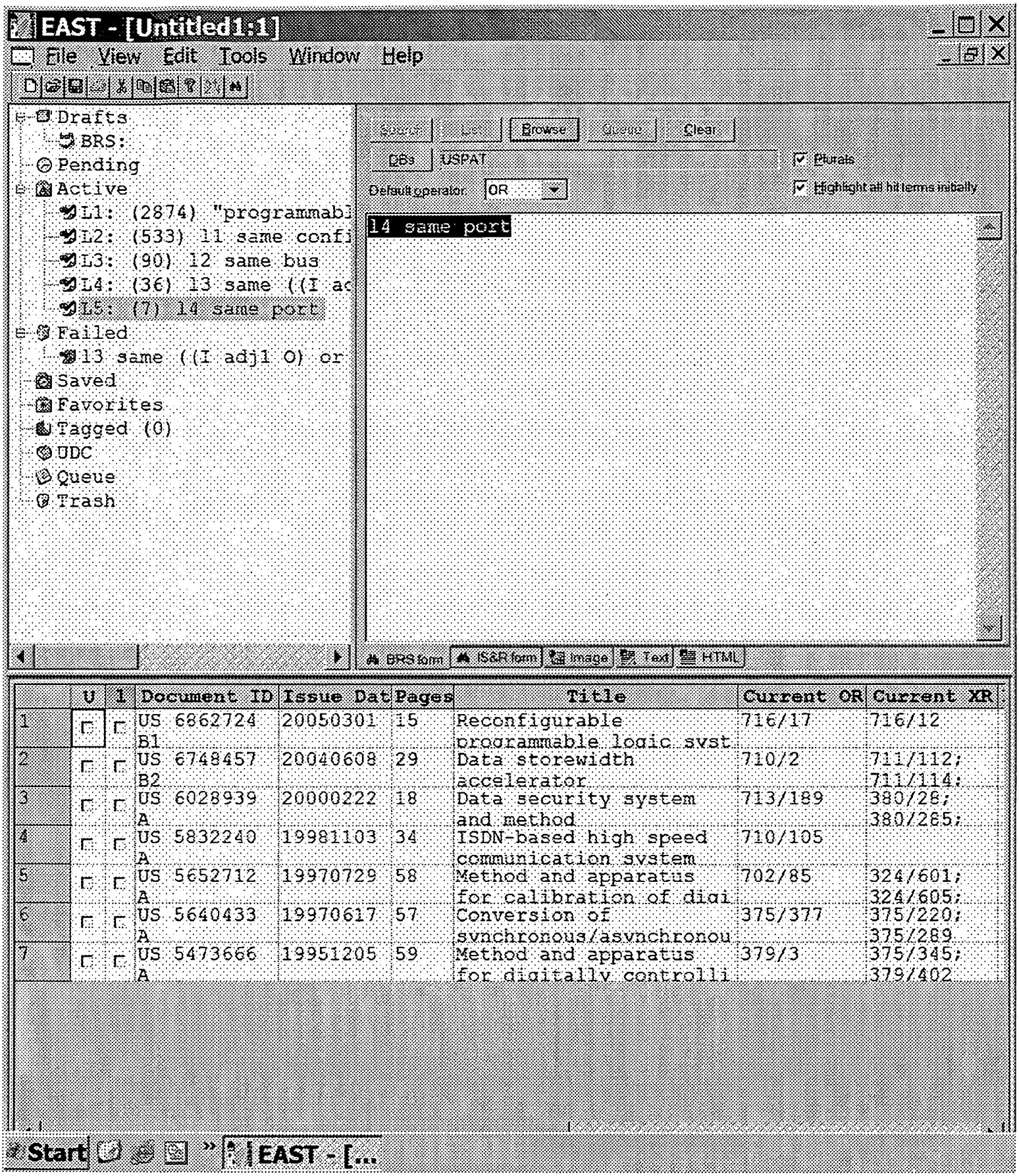
ATTY-AGENT-FIRM: Wolf, Greenfield & Sacks, P.C.

ABSTRACT:

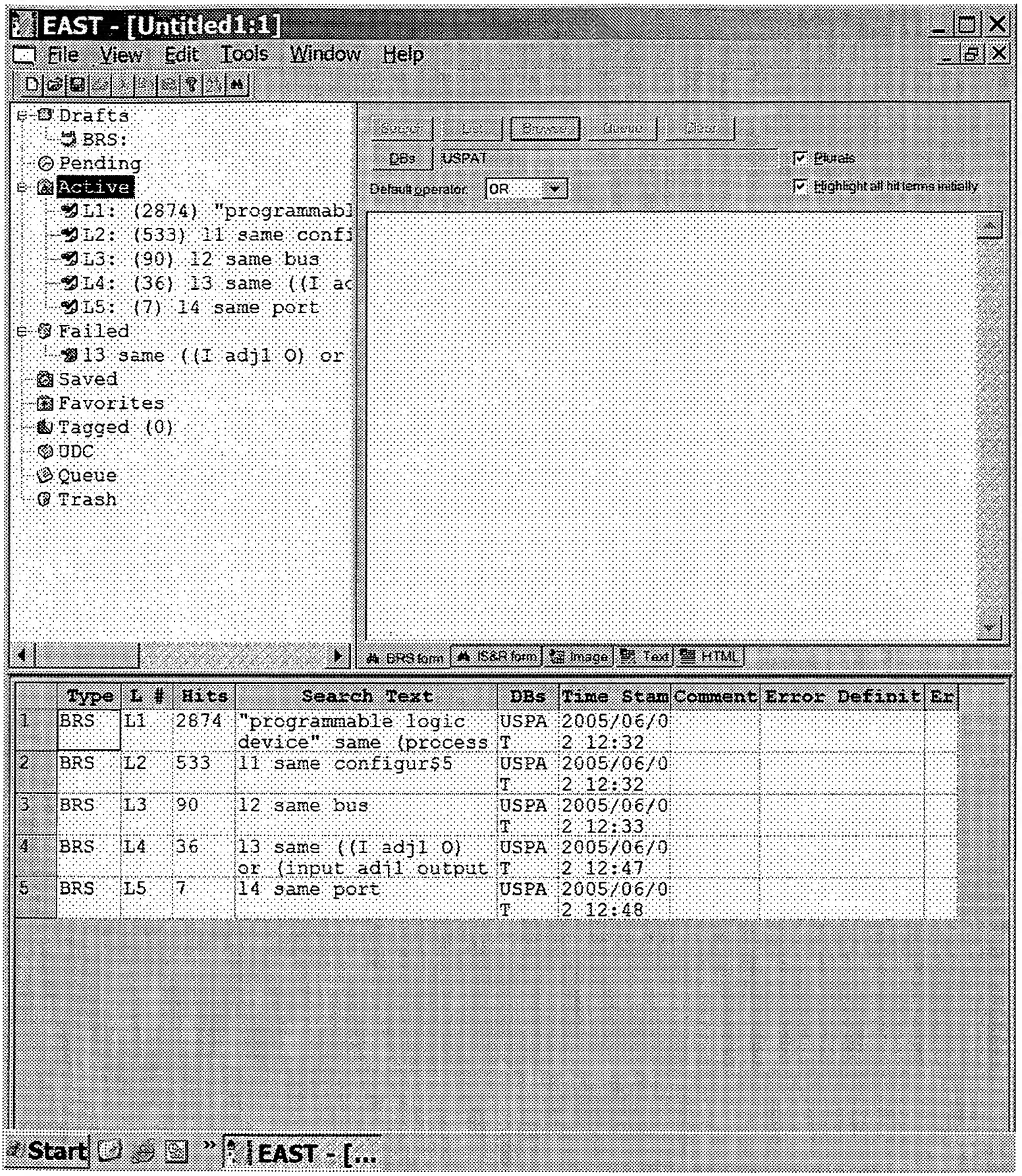
An interface device presents a generic serial input/output (I/O) port, whose function is programmable according to a stored sequence of instructions executed by a programmable state machine. The instructions cause the programmable state machine to define operation of the serial I/O port according to a standard or other predetermined set of serial I/O communication parameters.

17 Claims, 5 Drawing figures

Previous Doc Next Doc Go to Doc#



	U	1	Document ID	Issue Dat	Pages	Title	Current OR	Current XR
1	☐	☐	US 6862724 B1	20050301	15	Reconfigurable programmable logic syst	716/17	716/12
2	☐	☐	US 6748457 B2	20040608	29	Data storewidth accelerator	710/2	711/112; 711/114;
3	☐	☐	US 6028939 A	20000222	18	Data security system and method	713/189	380/28; 380/285;
4	☐	☐	US 5832240 A	19981103	34	ISDN-based high speed communication system	710/105	
5	☐	☐	US 5652712 A	19970729	58	Method and apparatus for calibration of digi	702/85	324/601; 324/605;
6	☐	☐	US 5640433 A	19970617	57	Conversion of synchronous/asynchronou	375/377	375/220; 375/289
7	☐	☐	US 5473666 A	19951205	59	Method and apparatus for digitally controlli	379/3	375/345; 379/402



	Type	L #	Hits	Search Text	DBs	Time Stam	Comment	Error Definit	Er
1	BRS	L1	2874	"programmable logic device" same (process	USPAT	2005/06/02 12:32			
2	BRS	L2	533	11 same configur$5	USPAT	2005/06/02 12:32			
3	BRS	L3	90	12 same bus	USPAT	2005/06/02 12:33			
4	BRS	L4	36	13 same ((I adj1 0) or (input adj1 output	USPAT	2005/06/02 12:47			
5	BRS	L5	7	14 same port	USPAT	2005/06/02 12:48			

US-PAT-NO: 5664198

DOCUMENT-IDENTIFIER: US 5664198 A

TITLE: High speed access to PC card memory using interrupts

---------- KWIC ----------

Abstract Text - ABTX (1):

A system for accessing attribute memory on a card using the interrupt capability of a microcontroller on the PCMCIA card intended to perform I/O functions for the host. The attribute memory interfaces directly with the microcontroller. A PLD is connected between the host bus and the microcontroller decodes the host's bus signals and generates an interrupt signal when it detects a request for access to the attribute memory which signal is supplied to the microcontroller. Upon receipt of the interrupt signal, the microcontroller runs a special routine that accesses attribute memory and supplies the results to the host. The PCMCIA card has a configured state in which the host has read the configuration information from attribute memory and has allocated necessary system resources. The PCMCIA card is in an unconfigured state if the foregoing has not been accomplished. The programmable logic device contains an AND gate having one of its inputs connected to the lines of the bus relating to the I/O function and a second input connected to the microprocessor for receiving a card enable signal, having at least two logic states. The control signals are passed to the microcontroller when the card enable signal is in one of the two logic states. The method consists of the steps of decoding the bus signals; when the host requests access to attribute memory, generate an interrupt signal and supply it to the microcontroller; the microcontroller runs an interrupt routine that includes saving the microcontroller registers, disabling the I/O functions, accessing the attribute memory, and providing the results to the host.

Brief Summary Text - BSTX (16):

These and other objects of the invention are achieved in a system for accessing attribute memory located on an add-in PC card. The attribute memory interfaces directly with a microcontroller also located on the PC card. The PC card operates within a host computer which includes a bus having address, data and control lines, and a microprocessor that supports interrupts. A programmable logic device is connected between the host bus and the microcontroller. The programmable logic device decodes the host's bus signals and generates an interrupt when it detects that the host has requested access to the attribute memory located on the PC card. The microcontroller then runs an interrupt routine that accesses attribute memory and supplies the results to the host. The interrupt is preferably a non-maskable interrupt although maskable interrupt is an alternative. The PC card may conform to the PCMCIA standard in which case configuration information is contained in the attribute memory. The PC card is intended to perform at least one I/O or memory function and has a configured state in which the host has read the configuration

US005664198A

United States Patent [19]

Chen et al.

[11] Patent Number: 5,664,198

[45] Date of Patent: Sep. 2, 1997

[54] HIGH SPEED ACCESS TO PC CARD MEMORY USING INTERRUPTS

[75] Inventors: Chengwu Chen; Michael E. Pierce; James L. Foote, III; all of Sacramento, Calif.

[73] Assignee: Intel Corporation, Santa Clara, Calif.

[21] Appl. No.: 329,230

[22] Filed: Oct. 26, 1994

[51] Int. Cl.[6] G06F 13/14; G06F 13/00

[52] U.S. Cl. 395/733; 395/651; 395/652

[58] Field of Search 395/733, 735, 395/775, 280, 375, 311, 846, 651, 652, 309, 427, 828

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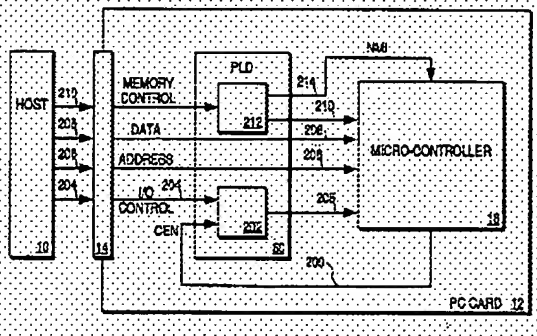
Primary Examiner—Gopal C. Ray
Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

[57] ABSTRACT

A system for accessing attribute memory on a card using the interrupt capability of a microcontroller on the PCMCIA card intended to perform I/O functions for the host. The attribute memory interfaces directly with the microcontroller. A PLD is connected between the host bus and the microcontroller decodes the host's bus signals and generates an interrupt signal when it detects a request for access to the attribute memory which signal is supplied to the microcontroller. Upon receipt of the interrupt signal, the microcontroller runs a special routine that accesses attribute memory and supplies the results to the host. The PCMCIA card has a configured state in which the host has read the configuration information from attribute memory and has allocated necessary system resources. The PCMCIA card is in an unconfigured state if the foregoing has not been accomplished. The programmable logic device contains an AND gate having one of its inputs connected to the lines of the bus relating to the I/O function and a second input connected to the microprocessor for receiving a card enable signal having at least two logic states. The control signals are passed to the microcontroller when the card enable signal is in one of the two logic states. The method consists of the steps of decoding the bus signals; when the host requests access to attribute memory, generate an interrupt signal and supply it to the microcontroller; the microcontroller runs an interrupt routine that includes saving the microcontroller registers, disabling the I/O functions, accessing the attribute memory, and providing the results to the host.

9 Claims, 3 Drawing Sheets



US-PAT-NO: 6252419

DOCUMENT-IDENTIFIER: US 6252419 B1

TITLE: LVDS interface incorporating phase-locked loop circuitry for use in programmable logic device

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Detailed Description Text - DETX (34):

FIG. 5 illustrates a programmable logic device 10 incorporating programmable I/O circuits 20 or 40 configured according to this invention in a data processing system 500. Data processing system 500 may include one or more of the following components: a processor 501; memory 502; I/O circuitry 503; and peripheral devices 504. These components are coupled together by a system bus 505 and are populated on a circuit board 506 which is contained in an end-user system 507.

US006252419B1

(12) **United States Patent**
Sung et al.

(10) **Patent No.: US 6,252,419 B1**
(45) **Date of Patent: Jun. 26, 2001**

(54) **LVDS INTERFACE INCORPORATING PHASE-LOCKED LOOP CIRCUITRY FOR USE IN PROGRAMMABLE LOGIC DEVICE**

(75) Inventors: Chiakang Sung, Milpitas; Beomki I. Wang, Cupertino; Richard G. Cliff, Milpitas, all of CA (US)

(73) Assignee: Altera Corporation, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/348,466

(22) Filed: Aug. 4, 1999

Related U.S. Application Data

(60) Provisional application No. 60/115,215, filed on Jan. 8, 1999.

(51) Int. Cl.[7] H03K 19/173; H03K 3/02; H03L 7/06

(52) U.S. Cl. 326/38; 326/38; 326/39; 326/40; 326/41; 327/156; 327/198

(58) Field of Search 326/37, 38, 39, 326/40, 41

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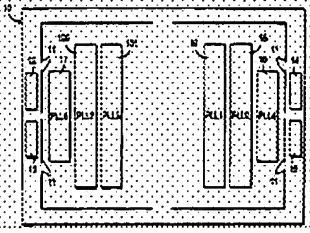
Primary Examiner—Michael Tokar
Assistant Examiner—Vibol Tan
(74) *Attorney, Agent, or Firm*—Fish & Neave; Jeffrey H. Ingerman

(57) **ABSTRACT**

An LVDS interface for a programmable logic device uses phase-locked loop ("PLL") circuits to provide data clocks for data input and output. The PLL clocks are highly accurate and each includes a multiply-by-W counter so that a multiplied and an unmultiplied clock are available. The multiplied clock is used to clock data into or out of a shift register chain serially. The unmultiplied clock is used to load or read the registers in the shift register chain in parallel. Providing both the multiplied and unmultiplied clocks from a single PLL assures that the clocks are in proper phase relationship so that the serial inputting or outputting, and the parallel loading or unloading, are properly synchronized.

44 Claims, 6 Drawing Sheets



US006262596B1

(12) **United States Patent**
Schultz et al.

(10) **Patent No.: US 6,262,596 B1**
(45) **Date of Patent: Jul. 17, 2001**

(54) **CONFIGURATION BUS INTERFACE CIRCUIT FOR FPGAS**

(75) Inventors: **David P. Schultz**, Lawrence C. Hung, both of San Jose; **F. Erich Goetting**, Cupertino, all of CA (US)

(73) Assignee: **Xilinx, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/374,471**

(22) Filed: **Aug. 13, 1999**

Related U.S. Application Data

(60) Provisional application No. 60/127,850, filed on Apr. 5, 1999.

(51) Int. Cl.[7] H03K 19/177

(52) U.S. Cl. 326/41; 326/39; 326/38; 326/40; 365/189.05

(58) Field of Search 326/36–41; 365/189.05

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Xilinx Application Note XAPP 151 version 1.1 entitled, "Virtex Configuration Architecture Advanced User's Guide", published Jul. 27, 1999, available from Xilinx Inc., 2100 Logic Drive, San Jose, California 95124.

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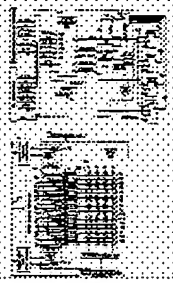
Primary Examiner—Michael Tokar
Assistant Examiner—Vibol Tan
(74) *Attorney, Agent, or Firm*—Patrick T. Bever; Lois D. Cartier

(57) **ABSTRACT**

A bus interface circuit for a programmable logic device (PLD) including an interface multiplexer connected between two or more external communication circuits and a configuration memory array. The interface multiplexer coordinates communication between a selected one of the external communication circuits and a packet processor. The packet processor interprets command/data information transmitted in a bit stream from the selected external communication circuit. In a default state, the interface multiplexer connects dual-purpose input/output pins of the PLD to the packet processor. In an alternative state, the interface multiplexer connects a JTAG interface circuit to the packet processor to facilitate configuration operations through the JTAG pins of the PLD.

19 Claims, 13 Drawing Sheets



US-PAT-NO: 5473666

DOCUMENT-IDENTIFIER: US 5473666 A
See image for Certificate of Correction

TITLE: Method and apparatus for digitally controlling gain in a talking path

--------- KWIC ---------

Detailed Description Text - DETX (25):
FIG. 4 illustrates the details of the CPU module 56. As noted on the left of FIG. 4, the bus 100a, 100b is shown connected from a processor 122 and extended to the programmable logic devices comprising the multi-path multiplexers 98 and 101 of the I/O module 50. In the preferred form of the invention, the processor 122 comprises a Motorola 68302 microprocessor operating at 16.67 MHz. The processor 122 accommodates three synchronous/asynchronous programmable serial ports. One serial port 124 can transmit or receive serial data between the test system 10 and the 201 XL translator 40 via the communication module 35 (FIG. 1). Port 124 accommodates synchronous serial data. The second serial port 126 accommodates asynchronous data from either remote HV modules or remote SS metallic test access unit (MTAU) modules. The third serial port 128 is an asynchronous port for communicating with the local craft interface 94 (FIG. 3). The serial ports 124-126 are multi-functional ports operating at the TTL level and are configurable to operate in transmit or receive modes based on the logic state of the RTU-DIS processor input 130. As noted above, the processor 122 is supported by numerous types of memory as shown in FIG. 4, and identified above. A number of address and data buffers 132 buffer signals on the unidirectional outgoing address bus 134, as well as the bidirectional data bus 136. System reset, enable and read/write signal lines 138 are carried throughout the internal system bus with the address and data signals. An additional bus 140 is connected to the digital signal processor module 58 for interrupt and acknowledge functions. A failure of the CPU module 56 is communicated to the I/O module 10 by way of the signal line 142.

US-PAT-NO: 5832240

DOCUMENT-IDENTIFIER: US 5832240 A

TITLE: ISDN-based high speed communication system

---------- KWIC ----------

Detailed Description Text - DETX (5):

The protocol processor 44, application processor 46 and PC bus can all interrupt each other using programmable input/output (I/O) pins. Protocol processor interrupts are also used by I/O circuits described below as indicators for transferring data between the PC card 30 and the ISDN network 16. Programmable chip selects on the protocol processor 44 are used to select DRAMs located in the shared memory 40. The protocol processor 44 preferably has access to the first megabyte of the shared memory 40. The programmable chip selects are also used to select serial communication circuits 48 and 50, and to select flash read only memories (ROMs) 52 and 54. Programmable I/O bits in 62 are used to generate and clear interrupts to and from the PC and the applications processor 46. The protocol processor 44 also comprises eight programmable I/O port bits for performing such functions as controlling a diagnostic light emitting diode (LED), reading the status of interrupts to the PC and the applications processor 46, and enabling the PC serial port. Processor 44 allows autobauding for rate adaption or, optionally, for a Non-Maskable Interrupt (NMI). A second timer provides a clock for the refresh rate timer in the DMA/interrupt/refresh controller 64. A third timer is used by the protocol processor as a real time clock. Programmable logic devices (PLDs) for implementing functions 60, 62, 66 and 68 are provided on the PC card and configured to control bus operations, and port configuration and I/O operations, memory, control and arbitration, respectively. The PLDs provide control signals for controlling and enabling the address and data bus buffers associated with the applications processor 46, protocol processor 44, and PC bus interface.

US005832240A

United States Patent [19]

Larsen et al.

[11] Patent Number: 5,832,240

[45] Date of Patent: Nov. 3, 1998

[54] ISDN-BASED HIGH SPEED COMMUNICATION SYSTEM

[76] Inventors: Allen J. Larsen; Jennifer K. Herget, both of 1300 Nadine Dr., Campbell, Calif. 95008; Charles D. Brown, 2206 Wildmere Pl., Herndon, Va. 22021; William C. Cross, 18549 Blythewood Dr., Los Gatos, Calif. 95030; Ronald E. Dove, 1511 Pool Dr., Felton, Calif. 95018; Paul W. T. Heller, 3765 Cefalu Dr., San Jose, Calif. 95124

[21] Appl. No.: 843,114

[22] Filed: Apr. 28, 1997

Related U.S. Application Data

[63] Continuation of Ser. No. 585,677, Jan. 11, 1996, abandoned, which is a continuation of Ser. No. 225,677, Apr. 11, 1994, abandoned, which is a division of Ser. No. 853,852, May 15, 1992, abandoned.

[51] Int. Cl.[6] G06F 13/00

[52] U.S. Cl. 395/283

[58] Field of Search 395/290, 285, 395,296; 370/64.1, 110.1; 379/211

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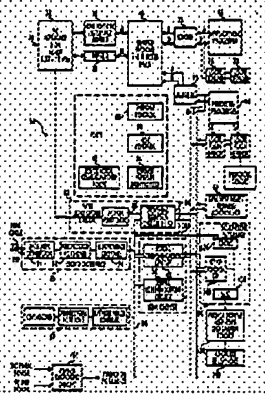
Primary Examiner—Ayaz R. Sheikh
Assistant Examiner—David A. Wiley
Attorney, Agent, or Firm—James R. Burdett

[57] ABSTRACT

An ISDN interface is provided on a card, which is adapted for mounting in a terminal computer and which is operable to exchange data with a terminal computer and an ISDN. The ISDN interface card includes a protocol processor that is programmable to process data encoded in accordance with a number of different protocols and a digital signal processor that is programmable for data compression, encryption and facsimile applications, and a-law and u-law conversion, among other applications. The ISDN card dynamically allocates data cells between one or two B-channels to achieve a data transmission rate of 128 kbps. A power supply with a ring generator is provided to allow for the use of an analog telephone with the ISDN card. The ISDN card is programmable to allow users to create customized screens for various call processes, and to allow for the updating of a flash ROM coupled to the protocol processor through the terminal computer and the ISDN.

22 Claims, 18 Drawing Sheets



US-PAT-NO: 6862724

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TITLE: Reconfigurable programmable logic system with peripheral identification data

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Brief Summary Text - BSTX (5):

More recently, programmable logic devices have been provided as part of systems that can include, separately or on the same chip, processors, memory, busses, UARTs, timers, various types of controllers, etc. In such programmable systems, the programmable logic device can be used to provide specialized user-designed logic functions, or it can be configured as one or more peripheral devices, such as modems, network interfaces, ports of various types, etc. If the programmable logic device is large enough, it can be configured to have a plurality of functions including both peripheral devices and user logic.

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(12) **United States Patent**
Riley et al.

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(54) **RECONFIGURABLE PROGRAMMABLE LOGIC SYSTEM WITH PERIPHERAL IDENTIFICATION DATA**

(75) Inventors: Paul Riley, Burntisland (GB); Clive Davies, Cumnor (GB); Iain Scott, Witney (GB); Chris Beetmar, Headington (GB); Andrew Draper, Chesham (GB)

(73) Assignee: Altera Corporation, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 128 days.

(21) Appl. No.: 10/268,111

(22) Filed: Sep. 25, 2002

(51) Int. Cl.[7] G06F 13/50
(52) U.S. Cl. 716/17; 716/1,12
(58) Field of Search 719/327; 716/1, 716/12, 16-18; 710/14

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Primary Examiner—Thuan Do
(74) *Attorney, Agent, or Firm*—Fish & Neave IP Group of Ropes & Gray LLP; Jeffrey H. Ingerman

(57) **ABSTRACT**

A reconfigurable programmable logic system including a programmable logic device and an associated processor is configured using a configuration file including (a) instructions for configuring the programmable logic device to one or more peripherals to be used by the processor, and (b) a list of the peripherals to be configured in the programmable logic. The processor uses the peripheral data from the configuration file to load the appropriate drivers, create all necessary instances of the drivers and optionally to pass parameters for any necessary initial command after each driver is loaded. Optionally, each time the system is configured, any previously loaded drivers are first unloaded.

36 Claims, 7 Drawing Sheets